Design of a Low-Voltage EEG Detector Based on a Chopping Amplifier in CMOS 65-nm

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***Abstract*—This paper presents a design of an Electroencephalography (EEG) detector circuit powered by 1.2V using a CMOS 65-nm process. The circuit comprises two main blocks: a chopping amplifier and a bandpass filter bank. The latter was implemented using Gm-C technology. The chopping amplifier comprises two Miller amplifiers and two choppers. The g_m/I_D methodology is used in order to size transistors. The designed EEG detector can amplify brain signals in the order of microvolts by 100dB. The whole detector demands a current consumption of 543µA and 31164µm² of active area. The power supply rejection PSRR results in 130.05dB. The circuit can be used in a Brain-Computer Interface (BCI) for several applications.**

***Index Terms*—EEG detector, CMOS, 65nm, g_m/I_D, Gm-C Filter, Chopping Amplifier, Fully Differential, OA, OTA**

I. Introduction

Electroencephalography (EEG) is used to detect and analyse brain activity for several applications like clinical diagnosis of brain pathologies, research on cognitive processes and brain-computer interfaces, among others [1]. For instance, EEG allows users to interact with their environment using only brain activity detection. This is achieved by means of a BCI that comprises an analogue part, the EEG detector, followed by a Analogue-to-Digital (A/D) converter and a digital processor. Its block diagram is shown in figure 1. The whole system transforms brain signals into commands, which can be used to turn on/off lights, to open/close doors or even to emulate a joystick of a video game. In agreement with different emotional states, brain signals are grouped in three frequency bands, namely: Alpha (8 Hz to 14 Hz), Beta (15 Hz to 31 Hz) and Gamma (32 Hz to 100 Hz). Their amplitudes range from a few to hundreds of microvolts. Thus, the use of ultra-sensitive electrodes disposed on the head is mandatory. The signal at the output of the electrodes must be amplified within those three frequency bands. On the one hand, in view of an efficient A/D conversion it is necessary to have at least 100 mV at the output of the EEG detector. This leads to a 100 dB total gain needed from the electrodes to the ADCs' inputs. On the other hand, since signals to amplify are much smaller than the operational amplifiers' (OA) offsets, traditional OA-based Instrumentation Amplifiers (IA) cannot be used. Indeed, the offset of an operational amplifier is commonly as high as 10 mV. If a classical IA is used, the input signal is masked by the OA's offset and noise that would be amplified by identical gain. In contrast, a chopping amplifier fits better the requirements of this application. By means of chopping modulation and filtering one can eliminate the OAs' offsets and the low-frequency noise [2].

In this work we design in CMOS 65-nm a multiple-output bandpass chopping amplifier that can be used as an EEG detector. The paper is structured as follows: firstly, the whole circuit is described and each block is explained in detail. Next, the design of each block is addressed, from the choice of the transistor parameters to the final circuit. The design methodology is explained in the third section. In section four, simulation results are discussed. Finally, conclusions are presented.

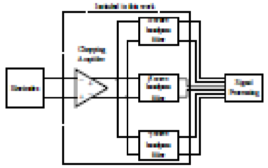

Fig. 1. Block diagram of an EEG acquisition system.

II. Circuit Description

Figure 1 shows a system-level view of the designed EEG detector that includes a chopping amplifier and three bandpass filters tuned at the central frequency of each band.

A. Chopping Amplifier

The chopping amplifier [2] shown in figure 2 comprises several parts: two 4-switch choppers, one at the input of a finite-gain fully differential amplifier and the other at its output. The amplifier is built from two identical single-ended operational amplifiers and its gain is set with four resistors. The chopping amplifier working principle can be described as follows:

1) the input signal is chopped at a given clock frequency in order to translate its baseband to higher frequencies
2) the chopping modulated signal is then amplified with an amplifier, and
3) the amplified signal is restored to its original baseband by chopping it again at the same clock frequency and phase.

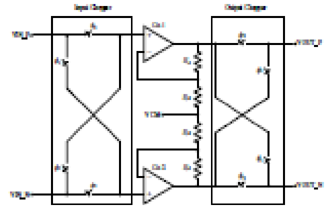

Fig. 2. Schematic of the chopping amplifier.

Since offset and low-frequency noise at the input of the fully-differential amplifier are chopped only once, their spectrums remain at high frequency and can be easily filtered out by low-frequency bandpass filters. The clock frequency must be high enough in order to avoid alias overlapping of the chopped modulated signal and to facilitate the filtering of modulated offset and noise. In this work we use a 10 kHz clock (50 % duty-cycle). Notice that we need two non-overlapping complementary clocks to ensure the good operation of the choppers. The closed loop-gain of the fully differential amplifier must be limited. Otherwise the OA's offset voltage (≈ 10 mV) will saturate the stage's output. For a 1.2 V supply this gain should be theoretically lower than 120. In this work, it was set at approximately 100 (40 dB). This can be attained by choosing the proper values for the resistors R_A and R_B in figure 2, as indicated in equation (1).

$$A_{closed} = (1 + \frac{R_A}{R_B}) = (1 + \frac{50\,k\Omega}{500\,\Omega}) = 101 \qquad (1)$$

B. Gm-C Filters

The signal at the output of the chopping amplifier must be filtered. As mentioned in the introduction, three bandpass filters are designed in the bands 8 Hz to 14 Hz, 15 Hz to 31 Hz and 32 Hz to 100 Hz. These, in turn, must further amplify the EEG signal, which is in the order of millivolts at the output of the chopping amplifier. To implement low-frequency analogue integrated filters, we considered the use of either switched-capacitor (SC) techniques or Gm-C filters implemented with operational transconductance amplifiers (OTA). However, for very low signal levels to amplify, continuous-time Gm-C filters are preferred because the switching noise, present everywhere in SC circuits, is avoided.

Each filter comprises three cascaded biquad sections. In fact, a simple bandpass filter has a slope of ±20 dB/decade, which is not enough for narrow bandpass realisations. Therefore, for each filter, the roll-off slopes are ±60 dB/decade in order to strongly attenuate the out-of-band signals. The total gain of each band filter at its centre frequency is almost 60dB. Figure 3 depicts the schematic of only one biquad section. All filters are fully-differential and have the same structure, but they differ in their central frequencies.

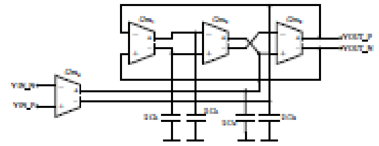

Fig. 3. Schematic of the biquad Gm-C section.

III. Circuit Design

The circuit was designed in a CMOS 65-nm process by means of the $\frac{g_m}{I_D}$ methodology and simulated with Spectre by using BSIM4 MOS transistor models.

A. Chopped Amplifier

For the OAs, two single-ended Miller amplifiers have been used. The value of the compensation capacitor was set to 3 pF in order to obtain the desired unity gain frequency ($f_T = 10$ MHz) and phase margin (60°). The f_T was chosen in order to obtain a closed loop-gain of 40 dB and a closed-loop bandwidth of 100 kHz. This bandwidth is needed because the chopped signal must be rebuilt at the output of the second chopper. Therefore, the amplifier must equally amplify at least ten harmonics of the chopped signal in order to minimise lineal signal distortion.

Actually, the Miller OA transfer function also presents a second non-dominant pole and one right half-plane (RHP) zero that introduce phase lag. In order to obtain a 60° phase margin, those singularities were placed far beyond the unity-gain frequency.

The choppers' switches are simply NMOS transistors. The amplitude of the clock signals was set to 1 V. The most important parameter of a switch is not the values of R_{on} and R_{off} separately but the ratio between them. To evaluate this ratio, the length of a transistor is set at the allowed minimum (0.14 µm in the CMOS 65 nm technology for transistors with very low VT) whereas the width was swept from 0.32 µm to 10 µm. As shown in figure 4 the ratio R_{off}/R_{on} increases quickly until saturation. Table I shows that the best result is obtained for $W = 10$ µm that gives rise to a R_{off}/R_{on} ratio of 226, approximately. It does not make sense to further increase the transistor width since the result would be almost identical.

TABLE I
Switch parameters, $W_1 = 0.32\,\mu m$ & $W_2 = 10\,\mu m$

W [µm]	R_{off} [Ω]	R_{on} [Ω]	R_{off}/R_{on}
0.32	[illegible]	[illegible]	[illegible]
10	15385	68	≈ 226

B. Gm-C Filters

Figure 3 shows the fully-differential Gm-C biquad section used for the filters. The transfer function of this bandpass section is given by:

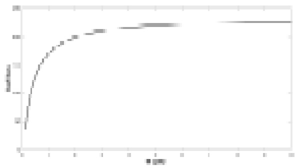

Fig. 4. $\frac{g_m I_D}{W}$ depending on the width of the NMOS transistor.

$$\frac{V_{out}}{V_{in}} = \frac{(\frac{G_{m4}}{C_B})s}{s^2 + (\frac{G_{m3}}{C_B})s + \frac{G_{m1}G_{m2}}{C_A C_B}} \quad (2)$$

In order to simplify the design and look at reusing as much as possible some of the filters' components, the following assumptions are made:

- $C_A = C_B = 1\,\mathrm{pF}$,
- $G_{m1} = G_{m2}$.

From the desired frequency response of the filter we can calculate the values of each G_m to be implemented. The smallest transconductance value is below 100 pS. For obtaining transconductances of this order of magnitude, the current division technique presented in [3] is used. The transconductor is shown in figure 5. Two composite NMOS mirrors can be noticed, each one comprising parallel (m) and series (n) connections of transistors.

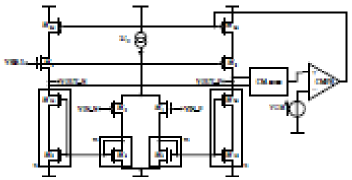

Fig. 5. Schematic of the transconductor $G_{m1\alpha}$.

The transconductance of this circuit is:

$$G_m = \frac{g_m}{I_D}\frac{I_D}{n.m} \quad (3)$$

where g_m is the small-signal transconductance of transistors M_0 and M_1 and I_D their drain currents. In view of a good matching, connecting transistors in parallel is better than increasing the number of fingers. Besides, the voltage supply must be high enough in order to warrant the correct operation of stacked transistors and the desired output swing. To this end, transistors are biased in weak inversion which ensures not only low current consumption but also small V_{ds} drops.

In equation (3) g_m/I_D is known because the weak inversion transistor operation is imposed ($g_m/I_D = q/n.k.T$). Parameters n and m were set to 10, except for $Gm_{2\beta}$ and $Gm_{3\gamma}$ in which n is set to one. The only unknown is I_D that can be calculated by means of the former equation. Then, with the help of the g_m/I_D curves, the transistors' sizes W/L are obtained [4].

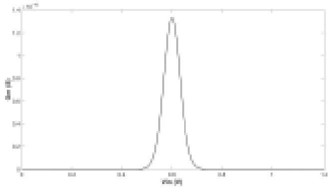

Fig. 6. DC sweep on transconductor $Gm_{1\alpha}$ to obtain its value at $VCM = 600\,\mathrm{mV}$.

For the input pair's tail current, a single PMOS transistor is used. Its width is set at the allowed minimum whereas its length was considerably increased in view of a high common-mode rejection of the transconductor itself.

For minimising phase errors that can lead to distorted filters' transfer function, the output impedance of the transconductor must be as high as possible. For this reason the PMOS active loads M_{34} and M_{35} must be cascoded by M_2 and M_3, respectively.

As in any fully-differential circuit, a common-mode feedback circuit (CMFB) is needed in order to set the DC voltages at the outputs of the transconductor [5]. These are set at $VCM = V_{DD}/2$ in order to allow the desired signal swing.

A DC sweep simulation permits the verification of the transconductance value of each transconductor. As shown in figure 6 G_m is measured at the common-mode voltage $VCM = 600\,\mathrm{mV}$, the DC level around which all signals evolve (the analogue ground). The transconductors' parameters are summarised in table II.

TABLE II
Gm-C FILTERS PARAMETERS

	Ideal [pS]	Simul. [pS]	I_D [nA]
$Gm_{1\alpha,3\alpha}$	13.299	13.306	0.6
$Gm_{2\alpha}$	75.4	75.4	0.38
$Gm_{4\alpha}$	701.46	701.45	6.5
$Gm_{1\beta,3\beta}$	27.271	27.272	2
$Gm_{2\beta}$	1791	1791	1
$Gm_{4\beta}$	1673.3	1673.46	1
$Gm_{1\gamma,3\gamma}$	111.98	111.96	6.5
$Gm_{2\gamma}$	174.12	174.11	10
$Gm_{4\gamma}$	7216	7215.97	6.5

IV. SIMULATION RESULTS

AC frequency response simulations on a Gm-C integrator allow us to measure the transconductors' phase error, which is the difference between the phase shift of an ideal integrator

TABLE III
OPEN-LOOP GAIN & PHASE ERROR OF EACH TRANSCONDUCTOR

	A_{v0} [dB]	Phase error [°]
$Gm_{1\alpha,3\alpha}$	38.42	0.57
$Gm_{2\alpha}$	38.85	0.88
$Gm_{4\alpha}$	33.80	0.78
$Gm_{1\beta,3\beta}$	43.58	0.52
$Gm_{2\beta}$	42.29	0.13
$Gm_{4\beta}$	46.35	0.13
$Gm_{1\gamma,3\gamma}$	36.01	0.83
$Gm_{2\gamma}$	38.66	0.16
$Gm_{4\gamma}$	35.07	0.2

($-90°$) and a real one at the unity-gain frequency. Simulation results for each transconductor are shown in table III. Notice that phase errors are kept below one degree, which is small enough to ensure undistorted filters' frequency response. Figure 7 shows the simulated frequency response of each filter including the gain of the chopping amplifier (40 dB).

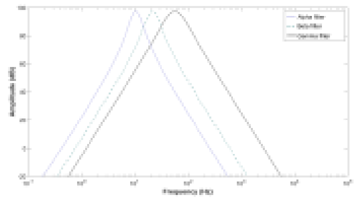

Fig. 7. Frequency response of each block.

The transient simulation is performed with a set of sinusoidal waves ranging from 5 Hz to 100 Hz in steps of 5 Hz. They are added to conform the input signal. The amplitude of each sinusoidal is 1 µV. Figure 8 shows the results of an FFT analysis of each filter's output. The envelope of the signals' spectrum analysis agrees with the filters' frequency response in figure 7.

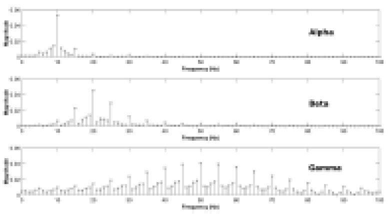

Fig. 8. FFT analysis of each output voltage.

The current consumption and active area occupied by the circuit are summarised in tables IV and V respectively. The chopping amplifier is the most power consuming block, this is because it requires large bandwidth Miller amplifiers ($f_T = 10\,\mathrm{MHz}$) that leads to bias three OA's transistors in strong inversion. The total active area is 31 164 µm^2.

TABLE IV
CURRENT CONSUMPTION OF EACH BLOCK

	Minimum [µA]	Maximum [µA]	RMS [µA]
Chopping amplifier	339.9	341.2	340
α filter	0.036	0.088	0.076
β filter	1.589	1.588	1.588
γ filter	1.737	1.756	1.736
Total	343.3	344.6	343.4

TABLE V
ACTIVE AREA OCCUPIED BY EACH BLOCK

Block	Subblock	Area [µm²]
Chopping amplifier	OAs	6 636.836
	Switchs	11.2
	Resistors	16.23757
α, β, γ filters	Transconductors	8 035.3808
	Capacitors	22179.46157

Finally, the power supply rejection ratio ($PSRR$) at DC can be approximated by:

$$PSRR(dB) = 20\,log_{10}(\frac{\Delta V_{supply} A_v}{\Delta V_{out}}) \quad (4)$$

By powering the circuit with 1.2 V and 1.4 V, the DC simulations reveal a $PSRR$ of 130.05 dB.

V. CONCLUSION

We presented the design of a fully-differential bandpass chopping amplifier that can be used as an EEG detector in a BCI. The circuit comprises a chopping modulated finite-gain amplifier and three 3rd order Gm-C filters that can be powered by a battery or energy harvesting techniques. The obtained performance figures meet the requirements for the intended application. Some improvements can be envisaged however, namely, the optimisation of the Miller amplifiers which are the most power consuming blocks. With this aim, it is possible to lower the chopping frequency so as to reduce the required bandwidth for such amplifiers. Nevertheless, this solution will demand more filtering efforts as higher order filters will be needed. This is feasible, in terms of power consumption, because the designed biquad sections are ultra low-power. This research will move forward towards the design of the circuit layout looking at the fabrication of a prototype.

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